Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method, comprising:

synchronising start of cell times in input/output circuits with cell transmission periods in a cross-connection circuit,

transferring cells between said input/output circuits by said cross-connection circuit in cell transfer periods,

changing configurations of said cross-connection circuit between cell transfer periods in cross-connection configuration periods,

sending cells from a sending input/output circuit of said input/output circuits at start of cell times,

receiving said sent cells in said cross-connection circuit, ~~wherein changing configurations includes~~

oscillating ~~said configurations~~ between a loopback configuration and a no-transmission ~~configuration during a set up period,~~ configuration,

transferring the received cells back to said sending input/output circuit in said loopback configuration and not transferring the received cells back to said sending input/output circuit in said no-transmission configuration,

receiving back transferred cells in said sending input/output circuit during said loopback configuration,

checking said ~~received~~ cells transferred back during said loopback configuration in said sending input/output circuit for a transmission error, and

shifting an offset of said start cell times in case a transmission error occurred, until transferring back at least one cell is wholly carried out within a cell transfer period.

2. (Previously Presented) A method according to claim 1, wherein the shifting includes shifting said offset of start of cell times in said sending input/output circuit, respectively, to align the time sent cells from said sending input/output circuit are received in said cross-connection circuit.

3. (Previously Presented) A method according to claim 1, including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

4. (Currently Amended) A method according to claim 1, including calculating start of cell times based on a start of cell signal and said offset of said start of cell times, ~~serialising~~ serializing said cells, and sending said ~~serialised~~ serialized cells together with said start of cell signal at said start of cell times.

5. (Currently Amended) A method according to claim 1, including receiving transferred back cells, ~~de-serialising~~ de-serializing said cells and checking each cell for transmission errors.

6. (Currently Amended) A method according to claim 1, including receiving transferred back cells, ~~de-serialising~~ de-serializing said cells and evaluating a bit error indicator.

7. (Previously Presented) A method according to claim 3, wherein the shifting includes shifting said offset of start of cell times using an offset counter and changing said offset counter by an amount of clock cycles of said central clock signal.

8. (Previously Presented) A method according to claim 1, wherein the shifting includes shifting said offset of said start of cell times to a maximum without generating transmission errors, and shifting said offset of said start of cell times to a minimum without generating transmission errors.

9. (Previously Presented) A method according to claim 8, wherein the shifting includes setting said offset of said start of cell times in between said maximum and said minimum.

10. (Currently Amended) A packet switch comprising:

a plurality of port controllers each with a cell input port and a cell output port, and

cross-connection means including cell input ports and cell output ports connected to said cell output ports and cell input ports of said port controllers, respectively,

wherein a sending port controller of said port controllers comprises:

a start of cell signal generator for generating start of cell signals,

an offset controller for shifting a start of cell time based on said start of cell signal, and

an error detection means for detecting corrupt received cells, ~~and~~

wherein said cross-connection means comprises:

a configuration controller for controlling an oscillation between a loopback configuration and a no-transmission configuration of said cross-connection ~~means.~~ means and the offset controller is configured to adjust the start of cell time based on detected corrupt cells received during the loopback configuration.

11. (Previously Presented) A packet switch according to claim 10, further comprising a central clock generator for providing a central clock signal, wherein said start of cell signal generator, said offset controller, and said configuration controller each comprise an input port for said central clock signal.

12. (Currently Amended) A packet switch according to claim 10, wherein said sending port controller comprises a ~~serialiser~~ serializer and a ~~de-serialiser~~ de-serialize for ~~serialising~~ serializing cells to be sent and ~~de-serialising~~ de-serializing received cells.

13. (Previously Presented) A packet switch according to claim 10, wherein said cross-connection means comprise a N × N crossbar matrix, selectively connecting N cell input ports with N cell output ports.

14. (Previously Presented) A packet switch according to claim 13, wherein said loopback configuration is realised by a unit matrix and a no-transmission configuration is realised by a null matrix.

15. (Previously Presented) A packet switch according to claim 10, wherein said error detection means is a bit error indicator.

16. (Currently Amended) A method, comprising:

synchronizing start of cell times, in a packet switched network, for plural port controllers during a set up to allow configuration changes in a cross-connection circuit without disturbing cell transfers;

transferring cells between said port controllers by said cross-connection circuit in cell transfer periods;

changing configurations of said cross-connection circuit between cell transfer periods in cross-connection configuration periods;

sending cells from a sending port controller of said port controllers at start of cell times;

receiving said sent cells in said cross-connection ~~circuit,~~ circuit; ~~wherein changing configurations includes~~

oscillating ~~said configurations~~ between a loopback configuration and a no-transmission ~~configuration during a set up period;~~ configuration;

transferring the received cells back to said sending port controller in said loopback configuration and not transferring the received cells back to said sending port controller in said no-transmission configuration;

receiving back transferred cells in said sending port controller during said loopback configuration;

checking said ~~received~~ cells transferred back in said sending port controller for a transmission error; and

shifting an offset of said start cell times in case a transmission error occurred, until transferring back at least one cell is wholly carried out within a cell transfer period.

17. (Canceled)

18. (Previously Presented) A method according to claim 16, wherein the shifting includes shifting said offset of start of cell times in said sending port controller, respectively, to align the time sent cells from said sending input/output circuit are received in said cross-connection circuit.

19. (Previously Presented) A method according to claim 16, including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

20. (Currently Amended) A method, comprising:

synchronising start of cell times in a plurality of port controllers during a set up to allow configuration changes in a cross-connection circuit without disturbing cell transfers, the port controllers each having a cell input port and a cell output port, and the cross-connection circuit including cell input ports and cell output ports connected to said cell output ports and cell input ports of said port controllers, respectively,

wherein a sending port controller of said port controllers performs:

generating start of cell signals using a start of cell signal generator,

shifting a start of cell time based on said start of cell signal using an offset controller, and

detecting corrupt received cells using an error detector, and

wherein said cross-connection controls an oscillation between a loopback configuration and a no-transmission configuration of said cross-connection ~~means,~~ circuit, using a configuration ~~controller.~~ controller, and the shifting is based on the detecting of corrupt cells received during the loopback configuration.

21. (Previously Presented) A method according to claim 20, further comprising providing a central clock signal using a central clock generator, wherein said start of cell signal generator, said offset controller, and said configuration controller each comprise an input port for said central clock signal.

22. (New) A system, comprising:

a plurality of port controllers each having a cell input port and a cell output port; and

a cross connection matrix coupled to the cell input ports and the cell output ports of the plurality of port controllers, the cross connection matrix having a configuration controller configured to control an oscillation between a loopback configuration and a no transmission configuration, wherein a sending port controller of the plurality of port controllers comprises:

a start of cell signal generator configured to generate a start of cell signals;

an error detector configured to detect errors in cells received during the loopback configuration; and

an offset controller configured to shift a start of cell time based on detected errors in the cells received during the loopback configuration.

23. (New) The system of claim 22, further comprising a central clock generator wherein the start of cell signal generator, the offset controller, and the configuration controller are coupled to the central clock generator.

24. (New) The system of claim 22 wherein the sending port controller comprises a serializer configured to serialize cells to be sent and a de-serializer configured to de-serialize received cells.

25. (New) The system of claim 22 wherein the cross-connection matrix comprise a N × N crossbar matrix configured to selectively connect N cell input ports with N cell output ports.

26. (New) The system of claim 22 wherein the matrix is configured as a unit matrix in the loopback configuration and is configured as a null matrix in the no-transmission configuration.

27. (New) The system of claim 22 wherein the error detector comprises a bit error indicator.